Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (withdrawn): A semiconductor device comprising:

a semiconductor substrate, one which an active region is formed;

a plurality of wiring layers which are formed on said semiconductor substrate;

a first insulating layer containing carbon, said first insulating layer being formed at least between any adjacent two of said wiring layers; and

a second insulating layer comprising silicon, carbon and nitrogen, said second insulating layer being formed on said first insulating layer.

Claim 2 (withdrawn): A semiconductor device as set forth in claim 1, wherein said second insulating layer further comprises boron.

Claim 3 (withdrawn): A semiconductor device as set forth in claim 1 or 2, which further comprises an adhesion layer which comprises a high-melting point metal and a nitride thereof, said adhesion layer being formed in the interface between said first insulating layer and said wiring layers.

Claim 4 (cancelled)

Claim 5 (currently amended): A method of manufacturing a semiconductor device~~, said method~~ comprising the steps of:

forming a wiring layer on a semiconductor substrate having an active region formed thereon;

forming a first insulating layer containing carbon on said wiring layer;

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forming a second insulating layer comprising silicon, carbon and nitrogen on said first insulating layer;

~~adding boron to said second insulating layer;~~

selectively etching said second insulating layer to form a first hole portion therethrough ~~until the surface of said first insulating layer is partially exposed~~;

selectively etching said first insulating layer with plasma to form a second hole portion therethrough, using said selectively-etched second insulating layer as a first mask pattern;

further selectively etching said second insulating layer to form a first groove portion therethrough;

further selectively etching said first insulating layer with plasma to form a second groove portion therethrough, using said further selectively-etched second insulating layer as a second mask pattern; and

forming a new wiring layer on said second insulating layer after selectively etching said first insulating layer, said hole portions and groove portions being filled with a material of said new wiring layer.

Claim 6 (currently amended): The method of ~~manufacturing a semiconductor device as set forth in~~ claim 5, wherein said step of selectively etching said second insulating layer is carried out with the plasma of the gas of a compound containing carbon and fluorine.

Claim 7 (currently amended): The method of ~~manufacturing a semiconductor device as set forth in~~ claim 5, wherein said step of selectively etching said second

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insulating layer is carried out with the plasma of the gas of a compound containing carbon and hydrogen.

Claim 8 (currently amended): The method of ~~manufacturing a semiconductor device as set forth in~~ claim 5, wherein said step of selectively etching said first insulating layer is carried out with the plasma of an oxygen-containing gas.

Claim 9 (currently amended): The method of ~~manufacturing a semiconductor device as set forth in~~ claim 5, wherein said step of selectively etching said first insulating layer is carried out with the plasma of a hydrogen-containing gas.

Claim 10 (new): The method of claim 5, wherein said step of further selectively etching said second insulating layer is carried out with the plasma of the gas of a compound containing carbon and fluorine.

Claim 11 (new): The method of claim 5, wherein said step of further selectively etching said second insulating layer is carried out with the plasma of the gas of a compound containing carbon and hydrogen.

Claim 12 (new): The method of claim 5, wherein said step of further selectively etching said first insulating layer is carried out with the plasma of an oxygen-containing gas.

Claim 13 (new): The method of claim 5, wherein said step of further selectively etching said first insulating layer is carried out with the plasma of a hydrogen-containing gas.

Claim 14 (new): The method of claim 5, further comprising adding boron to said second insulating layer.

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Claim 15 (new): The method of claim 5, wherein said hole portions and said groove portions at least partially overlap.

Claim 16 (new): A method of manufacturing a semiconductor device comprising:

forming a wiring layer on a semiconductor substrate having an active region formed thereon;

forming a first insulating layer containing carbon on said wiring layer;

forming a second insulating layer comprising silicon, carbon and nitrogen on said first insulating layer;

selectively etching said second insulating layer until the surface of said first insulating layer is partially exposed;

selectively etching said first insulating layer with plasma, using said selectively-etched second insulating layer as a first mask pattern, until the wiring layer is partially exposed,

further selectively etching said second insulating layer to expose more of the surface of said first insulating layer;

further selectively etch said first insulating layer with plasma, using said selectively-etch second insulating layer as a second mask pattern, without substantially exposing more wiring layer, and

forming a new wiring layer on said second insulating layer after selectively etching said first insulating layer, said hole portions and groove portions being filled with a material of said new wiring layer.

Claim 17 (new): The method of claim 16, wherein at least one of said step of selectively etching said second insulating layer or said step of further selectively etching

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said second insulating layer is carried out with the plasma of the gas of a compound containing carbon and fluorine.

Claim 18 (new) The method of claim 16, wherein at least one of said step of selectively etching said second insulating layer or said step of further selectively etching said second insulating layer is carried out with the plasma of the gas of a compound containing carbon and hydrogen.

Claim 19 (new) The method of claim 16, wherein at least one of said step of selectively etching said first insulating layer or said step of further selectively etching said first insulating layer is carried out with the plasma of an oxygen-containing gas.

Claim 20 (new) The method of claim 16, wherein at least one of said step of selectively etching said first insulating layer or said step of further selectively etching said first insulating layer is carried out with the plasma of a hydrogen-containing gas.

Claim 21 (new) The method of claim 16, further comprising adding boron to said second insulating layer.

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REMARKS

Applicants submit the Amendment, Petition for Extension of Time, and Request for Continued Examination in reply to the Final Office Action dated January 23, 2003 and Advisory Action dated March 26, 2003.

In this Amendment, Applicants have amended claim 5, 6-9 and 10-22 to more clearly define the invention. Claims 5 and 16 are the sole independent claims.

Before entry of this Amendment, claims 5-9 were pending in this application. After entry of this Amendment, claims 5-22 are pending in this application.

The originally-filed specification, claims, abstract, and drawings fully support the amendment to independent claim 5 and the subject matter of new claims 10-22. Specifically, the amendment to independent claim 5, the subject matter of new dependent claim 15, and the subject matter of new independent claim 16 are supported at least by Figs. 2(a)-2(f) and page 9, line 34 through page 12, line 8 of the specification. The subject matter of new claims 10-14 and 17-22 are supported at least by originally-filed claims 5-9. No new matter was introduced.

In the last Advisory Action, the Examiner maintained the rejection of 8 under 35 U.S.C. § 103(a) as being unpatentable over Zhao et al. (U.S. Patent No. 6,100,184) ("Zhao") in view of Moore et al. (U.S. Patent No. 6,251,802) ("Moore"), maintained the rejection of claim 5 under 35 U.S.C. § 103(a) as being unpatentable over Zhao in view of Moore and further in view of Fraser et al. (U.S. Patent No. 4,244,799) ("Fraser"), maintained the rejection of claims 6 and 7 under 35 U.S.C. § 103(a) as being unpatentable over Zhao in view of Moore and further in view of Wolf et al. ("Wolf"), and maintained the rejection of claim 9 under 35 U.S.C. § 103(a) as being unpatentable over

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Zhao in view of Moore and further in view of Chen et al. (U.S. Patent No. 6,211,061) ("Chen"). Applicants respectfully traverse the rejections.

No proper combination of the cited references, including Zhao, Moore, Fraser, Wolf, Chen, and the other art of record, teaches or suggests the present invention as claimed in independent claim 5.

For example, independent claim 5 recites a method of manufacturing a semiconductor device reciting, among other things, "selectively etching said second insulating layer to form a first hole portion; selectively etching said first insulating layer with plasma to form a second hole portion therethrough, using said selectively-etched second insulating layer as a first mask pattern; further selectively etching said second insulating layer to form a first groove portion therethrough," and "further selectively etching said first insulating layer with plasma to form a second groove portion therethrough, using said selectively-etch second insulating layer as a second mask pattern." No proper combination of the cited references teaches or suggest the aforementioned method steps either alone or in combination with the other method steps of the claimed invention.

Zhao discloses depositing an etch-stop layer 15 over a first low-dielectric constant dielectric layer 14, forming an opening 17 in the etch-stop layer 15, depositing a second low-dielectric constant dielectric layer 18 on the etch-stop layer 15, depositing a second etch-stop layer 19 on the second low-dielectric constant dielectric layer 18, forming an opening 23 in the etch-stop layer 19, and then etching the exposed regions of both the first and second low-dielectric constant dielectric layers 14, 18 underlying the openings 17, 23 of the etch-stop layers 15, 19. (Col. 5, line 53 through col. 7, line 45).

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Zhao does not disclose "selectively etching said second insulating layer to form a first hole portion; selectively etching said first insulating layer with plasma to form a second hole portion therethrough, using said selectively-etched second insulating layer as a first mask pattern; further selectively etching said second insulating layer to form a first groove portion therethrough," and "further selectively etching said first insulating layer with plasma to form a second groove portion therethrough, using said selectively-etch second insulating layer as a second mask pattern." Indeed, Zhao does not teach or suggest either "selectively etching" and "further selectively etching" any single layer, or "selectively etching" a "hole portion" and then "further selectively etching" a "groove portion" on any single layer. Accordingly, because Zhao does not teach or suggest the claimed invention, and neither Moore, Fraser, Wolf, nor Chen remedy the deficiencies of Zhao, Applicants respectfully request withdrawal of the rejection.

Applicant also submits that no proper combination of the cited references, including Zhao, Moore, Fraser, Wolf, Chen, and the other art of record, teaches or suggests the present invention as claimed in new independent claim 16.

Applicant further submits that dependent claims 6-15 and 17-22 are patentable over the cited references, including Zhao, Moore, Fraser, Wolf, Chen, and the other art of record. This is true whether such art is considered alone or in any proper combination, in particular, at least due to the dependency of claims 6-15, directly or indirectly, from independent claim 5, and the dependency of claims 17-22, directly or indirectly, from independent claim 16.

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In view of the foregoing amendments and remarks, Applicant respectfully requests the reconsideration and reexamination of this application and the timely allowance of the pending claims.

The Office Action contains characterizations of the claims and the related art with which Applicant does not necessarily agree. Unless expressly noted otherwise, Applicant declines to subscribe to any statement or characterization in the Office Action.

In discussing the specification, claims, abstract, and drawings in this Amendment, it is to be understood that Applicant is in no way intending to limit the scope of the claims to any exemplary embodiments described in the specification or abstract and/or shown in the drawings. Rather, Applicant is entitled to have the claims interpreted broadly, to the maximum extent permitted by statute, regulation, and applicable case law.

Please grant any extensions of time required to enter this response and charge any additional required fees to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, L.L.P.

Dated: July 23, 2003

By: _____

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